SEMICONDUCTOR MEMORY DEVICE

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CROSS REFERENCE TO RELATED APPLICATION

[01] This application is a continuation of prior U.S. patent application no. 09/964,851, filed September 28, 2001, which Now a U.S. Patent No. 6,617,651, claims the benefit of priority under 35 U.S.C. § 119 to Japanese Patent Application No. 2001-220461 filed on July 19, 2001, the entire contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[02] The present invention relates to a semiconductor memory device, specifically, to a semiconductor memory device having full depletion type MISFETs.

Related Background Art

[03] In a related DRAM, a memory cell is composed of an MOS transistor and a capacitor. The scale-down of the DRAM has been remarkably advanced by the adoption of a trench capacitor structure and a stacked capacitor structure. At present, the cell size of a unit memory cell is scaled down to an area of $2\ F \times 4\ F = 8\ F^2$, where F is a minimum feature